

In the Claims

This listing of claims will replace all prior versions and listings of claims in the application:

1 1. (Currently Amended) A method of generating an image
2 using raster image processing, said image being generated based
3 on a specification specifying said image, said specification
4 containing data representing a plurality of objects in a page,
5 said method comprising:

6 implementing a plurality of approaches, with each approach
7 being designed to generate said image;

8 receiving said specification;

9 examining said specification to determine a number of
10 resources required to generate said image of a page in each of
11 said plurality of approaches;

12 selecting one of said plurality of approaches which requires
13 an optimal number of resources;

14 generating said image of said page from said specification
15 using said selected one of said plurality of approaches.

2 to 4. (Canceled)

1 5. (Currently Amended) The method of claim 4 1, wherein:
2 said plurality of approaches includes rendering and
3 screening via back-end screening and rendering and screening via
4 pipelined screening; and

5 said examining comprises determining a minimum duration of
6 time consumed by either said back-end screening or said pipelined
7 screening.

1 6. (Original) The method of claim 5, wherein a system
2 implementing said method contains a random access memory (RAM)
3 and a cache, wherein said cache enables faster access to data to
4 a processing unit, said determining a minimum duration further
5 comprises determining an additional time required by said back-
6 end screening approach due to storing rendered data in said RAM.

1 7. (Original) The method of claim 5, wherein said
2 determining a minimum duration further comprises determining an
3 additional time required by said pipelined screening due to the
4 overlap of objects contained in said specification for said
5 image.

1 8. (Original) The method of claim 5, wherein a system
2 implementing said method contains a random access memory (RAM)
3 and a cache, wherein said cache enables faster access to data to
4 a processing unit, wherein said determining a minimum duration
5 further comprises determining an additional time required by said
6 pipelined screening when said processing unit accesses a code in
7 cache enabling implementation of said pipelined screening, and an
8 instruction cache miss results in accessing said code in said
9 cache.

1 9. (Original) The method of claim 5, wherein a system
2 implementing said method contains a random access memory (RAM)
3 and a cache, wherein said cache enables faster access to data to
4 a processing unit, said determining a minimum duration further
5 comprises determining an additional time required by said
6 pipelined screening if a data structure for a desired tile size
7 does not fit in said cache, wherein said data structure is used
8 in said pipelined screening.

10. (Canceled)

1 11. (Currently Amended) A system for generating an image
2 using raster image processing, said image being generated based
3 on a specification specifying said image, said specification
4 containing data representing a plurality of objects in a page,
5 said system comprising:

6 means for implementing a plurality of approaches, with each
7 approach being designed to generate said image;

8 means for receiving said specification;

9 means for examining said specification to determine a number
10 of resources required to generate said image of a page in each of
11 said plurality of approaches;

12 means for selecting one of said plurality of approaches
13 which requires an optimal number of resources;

14 means for generating said image of said page from said
15 specification using said selected one of said plurality of
16 approaches.

12 to 14. (Canceled)

1 15. (Currently Amended) The system of claim 14 11, wherein:
2 said plurality of approaches includes rendering and
3 screening via back-end screening and rendering and screening via
4 pipelined screening; and

5 said means for examining comprises means for determining a
6 minimum duration of time consumed by either said back-end
7 screening or said pipelined screening.

16. (Canceled)

1 17. (Currently Amended) A computer program product for use
2 with a computer system, said computer program product comprising
3 a computer usable medium having computer readable program code
4 means embodied in said medium generating an image using raster
5 image processing, said image being generated based on a
6 specification specifying said image, said specification
7 containing data representing a plurality of objects of a page,
8 said computer program product including:

9 computer readable program code means for implementing a
10 plurality of approaches, with each approach being designed to
11 generate said image;

12 computer readable program code means for receiving said
13 specification;

14 computer readable program code means for examining said
15 specification to determine a number of resources required to
16 generate said image of a page in each of said plurality of
17 approaches;

18 computer readable program code means for selecting one of
19 said plurality of approaches which requires an optimal number of
20 resources;

21 computer readable program code means for generating said
22 image of said page from said specification using said selected
23 one of said plurality of approaches.

18 to 20. (Canceled)

1 21. (Currently Amended) The computer program product of
2 claim 20 17, wherein:

3 said plurality of approaches includes rendering and
4 screening via back-end screening and rendering and screening via
5 pipelined screening; and

6 said computer readable program code means for examining
7 comprises computer readable program code means for determining a
8 minimum duration of time consumed by either said back-end
9 screening or said pipelined screening.

1 22. (New) The method of claim 5, wherein:

2 said determining a minimum duration of time consumed by
3 either said back-end screening or said pipelined screening
4 calculates CLK as follows:

5 $CLK = T_d - T_p - T_c$

6 where T_d is the additional time required for back-end
7 screening given by:

8 $T_d = (Pagesize \times DPSI) \times 2 / (\text{Transfer-rate})$

9 where: Pagesize is the area of the page; DPSI is the dots per
10 square inch; and Transfer-rate is a memory data transfer rate;
11 where T_p is the difference in screening performance between
12 pipeline screening and back-end screening given by:

13 $T_p = (\sum A_i \times DPSI \times CLK_p) - (Pagesize \times DPSI \times CLK_b)$

14 where: A_i is the bounding box area of i^{th} display list element i
15 in square inches; CLK_p is the average number clock cycles
16 required to process each pixel in pipeline screening; and CLK_b is

17 the average number clock cycles required to process each pixel in
18 back-end screening;

19 where T_c is the difference in cache misses between pipeline
20 screening back-end screening given by:

21

$$T_c = (\sum (I_n \times (C_{pi} - C_{bi}))) \times CLK_{cache}$$

22 where: I_n is the total number of element of type i in the display
23 list; C_{pi} is the number of cache misses in one rendering for an
24 element of type i in pipeline screening; C_{bi} is the number of
25 cache misses in one rendering for element type i in back-end
26 screening; and CLK_{cache} is the number of clock cycles required to
27 serve one cache miss.

1 23. (New) The method of claim 5, wherein:

2 said determining a minimum duration of time consumed by
3 either said back-end screening or said pipelined screening
4 employing a predetermined screen tile height in screening
5 calculates CLK as follows:

6

$$CLK = T_d - T_p - T_c - T_t$$

7 where T_d is the additional time required for back-end
8 screening given by:

9

$$T_d = (Pagesize \times DPSI) \times 2 / (Transfer-rate)$$

10 where: Pagesize is the area of the page; DPSI is the dots per
11 square inch; and Transfer-rate is a memory data transfer rate;

12 where T_p is the difference in screening performance between
13 pipeline screening and back-end screening given by:

14 $T_p = (\sum A_i \times DPSI \times CLK_p) - (\text{Pagesize} \times DPSI \times CLK_b)$

15 where: A_i is the bounding box area of i^{th} display list element i
16 in square inches; CLK_p is the average number clock cycles
17 required to process each pixel in pipeline screening; and CLK_b is
18 the average number clock cycles required to process each pixel in
19 back-end screening;

20 where T_c is the difference in cache misses between pipeline
21 screening back-end screening given by:

22 $T_c = (\sum (I_n \times (C_{pi} - C_{bi}))) \times CLK_{cache}$

23 where: I_n is the total number of element of type i in the display
24 list; C_{pi} is the number of cache misses in one rendering for an
25 element of type i in pipeline screening; C_{bi} is the number of
26 cache misses in one rendering for element type i in back-end
27 screening; and CLK_{cache} is the number of clock cycles required to
28 serve one cache miss; and

29 where: T_t is the number of excess clock cycles between
30 pipelined screening and back-end screening due to a screening
31 table not being able to fit in a cache when the object height is
32 less than the predetermined screen tile height given by:

33 $T_t = (\sum a_i \times DPSI) \times CLK_{tp}$

34 where: a_i is bounding box area of display list element i ; and
35 CLK_{tp} is the number of clock cycles to process a cache miss.

1 24. (New) The method of claim 5, wherein:
2 said determining a minimum duration of time consumed by
3 either said back-end screening or said pipelined screening
4 employing a predetermined screen tile height in screening
5 calculates CLK as follows:

6 $CLK = T_d - T_p - T_c - T_t$

7 where T_d is the additional time required for back-end
8 screening given by:

9 $T_d = (Pagesize \times DPSI) \times 2 / (\text{Transfer-rate})$

10 where: Pagesize is the area of the page; DPSI is the dots per
11 square inch; and Transfer-rate is a memory data transfer rate;

12 where T_p is the difference in screening performance between
13 pipeline screening and back-end screening given by:

14 $T_p = (\sum A_i \times DPSI \times CLK_p) - (Pagesize \times DPSI \times CLK_b)$

15 where: A_i is the bounding box area of i^{th} display list element i
16 in square inches; CLK_p is the average number clock cycles
17 required to process each pixel in pipeline screening; and CLK_b is
18 the average number clock cycles required to process each pixel in
19 back-end screening;

20 where T_c is the difference in cache misses between pipeline
21 screening back-end screening given by:

22 $T_c = (\sum (I_n \times (C_{pi} - C_{bi}))) \times CLK_{\text{cache}}$

23 where: I_n is the total number of element of type i in the display
24 C_{pi} is the number of cache misses in one rendering for an
25 element of type i in pipeline screening; C_{bi} is the number of
26 cache misses in one rendering for element type i in back-end
27 screening; and CLK_{cache} is the number of clock cycles required to
28 serve one cache miss; and

29 where: T_t is the number of excess clock cycles between
30 pipelined screening and back-end screening due to a screening
31 table not being able to fit in a cache when the object height is
32 greater than the predetermined screen tile height given by:

33
$$T_t = (\sum h_i \times DPSI \times T_w) \times CLK_{tp}$$

34 where: h_i is the height of display list element i ; T_w is the width
35 of the screen; and CLK_{tp} is the number of clock cycles to process
36 a cache miss.

1 25. (New) The system of claim 15, further comprising:
2 a random access memory (RAM); and
3 a cache, wherein said cache enables faster access to data to
4 a processing unit; and

5 wherein said means for determining a minimum duration
6 further comprises means for determining an additional time
7 required by said back-end screening approach due to storing
8 rendered data in said RAM.

1 26. (New) The method of claim 15, wherein:
2 said means for determining a minimum duration further
3 comprises means for determining an additional time required by
4 said pipelined screening due to the overlap of objects contained
5 in said specification for said image.

1 27. (New) The method of claim 15, further comprising:
2 a random access memory (RAM);
3 a cache, wherein said cache enables faster access to data to
4 a processing unit than said random access memory; and
5 wherein said means for determining a minimum duration
6 further comprises means for determining an additional time
7 required by said pipelined screening when said processing unit
8 accesses a code in cache enabling implementation of said
9 pipelined screening, and an instruction cache miss results in
10 accessing said code in said cache.

1 28. (New) The method of claim 15, further comprising:
2 a random access memory (RAM);
3 a cache, wherein said cache enables faster access to data to
4 a processing unit than said random access memory (RAM); and
5 wherein said means for determining a minimum duration
6 further comprises means for determining an additional time
7 required by said pipelined screening if a data structure for a
8 desired tile size does not fit in said cache, wherein said data
9 structure is used in said pipelined screening.

1 29. (New) The method of claim 15, wherein:
2 said determining a minimum duration of time consumed by
3 either said back-end screening or said pipelined screening
4 calculates CLK as follows:

5 $CLK = T_d - T_p - T_c$

6 where T_d is the additional time required for back-end
7 screening given by:

8 $T_d = (\text{Pagesize} \times \text{DPSI}) \times 2 / (\text{Transfer-rate})$

9 where: Pagesize is the area of the page; DPSI is the dots per
10 square inch; and Transfer-rate is a memory data transfer rate;
11 where T_p is the difference in screening performance between
12 pipeline screening and back-end screening given by:

13 $T_p = (\sum A_i \times \text{DPSI} \times \text{CLK}_p) - (\text{Pagesize} \times \text{DPSI} \times \text{CLK}_b)$

14 where: A_i is the bounding box area of i^{th} display list element i
15 in square inches; CLK_p is the average number clock cycles
16 required to process each pixel in pipeline screening; and CLK_b is
17 the average number clock cycles required to process each pixel in
18 back-end screening;

19 where T_c is the difference in cache misses between pipeline
20 screening back-end screening given by:

21 $T_c = (\sum (I_n \times (C_{pi} - C_{bi}))) \times \text{CLK}_{\text{cache}}$

22 where: I_n is the total number of element of type i in the display
23 list; C_{pi} is the number of cache misses in one rendering for an
24 element of type i in pipeline screening; C_{bi} is the number of
25 cache misses in one rendering for element type i in back-end
26 screening; and $\text{CLK}_{\text{cache}}$ is the number of clock cycles required to
27 serve one cache miss.

1 30. (New) The method of claim 15, wherein:

2 said determining a minimum duration of time consumed by
3 either said back-end screening or said pipelined screening

4 employing a predetermined screen tile height in screening
5 calculates CLK as follows:

6
$$CLK = T_d - T_p - T_c - T_t$$

7 where T_d is the additional time required for back-end
8 screening given by:

9
$$T_d = (\text{Pagesize} \times \text{DPSI}) \times 2 / (\text{Transfer-rate})$$

10 where: Pagesize is the area of the page; DPSI is the dots per
11 square inch; and Transfer-rate is a memory data transfer rate;

12 where T_p is the difference in screening performance between
13 pipeline screening and back-end screening given by:

14
$$T_p = (\sum A_i \times \text{DPSI} \times CLK_p) - (\text{Pagesize} \times \text{DPSI} \times CLK_b)$$

15 where: A_i is the bounding box area of i^{th} display list element i
16 in square inches; CLK_p is the average number clock cycles
17 required to process each pixel in pipeline screening; and CLK_b is
18 the average number clock cycles required to process each pixel in
19 back-end screening;

20 where T_c is the difference in cache misses between pipeline
21 screening back-end screening given by:

22
$$T_c = (\sum (I_n \times (C_{pi} - C_{bi}))) \times CLK_{\text{cache}}$$

23 where: I_n is the total number of element of type i in the display
24 list; C_{pi} is the number of cache misses in one rendering for an
25 element of type i in pipeline screening; C_{bi} is the number of
26 cache misses in one rendering for element type i in back-end

27 screening; and CLK_{cache} is the number of clock cycles required to
28 serve one cache miss; and

29 where: T_t is the number of excess clock cycles between
30 pipelined screening and back-end screening due to a screening
31 table not being able to fit in a cache when the object height is
32 less than the predetermined screen tile height given by:

33
$$T_t = (\sum a_i \times DPSI) \times CLK_{tp}$$

34 where: a_i is bounding box area of display list element i; and
35 CLK_{tp} is the number of clock cycles to process a cache miss.

1 31. (New) The method of claim 15, wherein:

2 said determining a minimum duration of time consumed by
3 either said back-end screening or said pipelined screening
4 employing a predetermined screen tile height in screening
5 calculates CLK as follows:

6
$$CLK = T_d - T_p - T_c - T_t$$

7 where T_d is the additional time required for back-end
8 screening given by:

9
$$T_d = (Pagesize \times DPSI) \times 2 / (\text{Transfer-rate})$$

10 where: Pagesize is the area of the page; DPSI is the dots per
11 square inch; and Transfer-rate is a memory data transfer rate;

12 where T_p is the difference in screening performance between
13 pipeline screening and back-end screening given by:

14
$$T_p = (\sum A_i \times DPSI \times CLK_p) - (Pagesize \times DPSI \times CLK_b)$$

15 where: A_i is the bounding box area of i^{th} display list element i
16 in square inches; CLK_p is the average number clock cycles
17 required to process each pixel in pipeline screening; and CLK_b is
18 the average number clock cycles required to process each pixel in
19 back-end screening;

20 where T_c is the difference in cache misses between pipeline
21 screening back-end screening given by:

22
$$T_c = (\sum (I_n \times (C_{pi} - C_{bi}))) \times CLK_{cache}$$

23 where: I_n is the total number of element of type i in the display
24 list; C_{pi} is the number of cache misses in one rendering for an
25 element of type i in pipeline screening; C_{bi} is the number of
26 cache misses in one rendering for element type i in back-end
27 screening; and CLK_{cache} is the number of clock cycles required to
28 serve one cache miss; and

29 where: T_t is the number of excess clock cycles between
30 pipelined screening and back-end screening due to a screening
31 table not being able to fit in a cache when the object height is
32 greater than the predetermined screen tile height given by:

33
$$T_t = (\sum h_i \times DPSI \times T_w) \times CLK_{tp}$$

34 where: h_i is the height of display list element i ; T_w is the width
35 of the screen; and CLK_{tp} is the number of clock cycles to process
36 a cache miss.

1 32. (New) A method of generating an image using raster
2 image processing, said image being generated based on a
3 specification specifying said image, said specification

4 containing data representing a plurality of objects in a page,
5 said method comprising:
6 implementing a plurality of approaches, with each approach
7 being designed to generate said image;
8 receiving said specification;
9 examining said specification to determine a number of
10 resources required to generate said image of a subset of a page
11 including plural objects in each of said plurality of approaches;
12 selecting one of said plurality of approaches which requires
13 an optimal number of resources;
14 generating said image of said page from said specification
15 using said selected one of said plurality of approaches.

1 33. (New) The method of claim 32, wherein:
2 said subset of a page including plural objects consists of a
3 band of a predetermined number of adjacent horizontal lines.

1 34. (New) The method of claim 32, wherein:
2 said subset of a page including plural objects consists of a
3 subband of a rectangle of a predetermined number of adjacent
4 pixels in a predetermined number of adjacent horizontal lines.

1 35. (New) The method of claim 32, wherein:
2 said plurality of approaches includes rendering and
3 screening via back-end screening and rendering and screening via
4 pipelined screening;
5 said examining comprises determining a minimum duration of
6 time consumed by either said back-end screening or said pipelined
7 screening; and
8 wherein a system implementing said method contains a random
9 access memory (RAM) and a cache, wherein said cache enables

10 faster access to data to a processing unit, said determining a
11 minimum duration further comprises determining an additional time
12 required by said back-end screening approach due to storing
13 rendered data in said RAM.

1 36. (New) The method of claim 32, wherein:
2 said plurality of approaches includes rendering and
3 screening via back-end screening and rendering and screening via
4 pipelined screening;

5 said examining comprises determining a minimum duration of
6 time consumed by either said back-end screening or said pipelined
7 screening; and

8 wherein said determining a minimum duration further
9 comprises determining an additional time required by said
10 pipelined screening due to the overlap of objects contained in
11 said specification for said image.

1 37. (New) The method of claim 32, wherein:
2 said plurality of approaches includes rendering and
3 screening via back-end screening and rendering and screening via
4 pipelined screening;

5 said examining comprises determining a minimum duration of
6 time consumed by either said back-end screening or said pipelined
7 screening; and

8 wherein a system implementing said method contains a random
9 access memory (RAM) and a cache, wherein said cache enables
10 faster access to data to a processing unit, wherein said
11 determining a minimum duration further comprises determining an
12 additional time required by said pipelined screening when said
13 processing unit accesses a code in cache enabling implementation

14 of said pipelined screening, and an instruction cache miss
15 results in accessing said code in said cache.

1 38. (New) The method of claim 32, wherein:
2 said plurality of approaches includes rendering and
3 screening via back-end screening and rendering and screening via
4 pipelined screening;

5 said examining comprises determining a minimum duration of
6 time consumed by either said back-end screening or said pipelined
7 screening; and

8 wherein a system implementing said method contains a random
9 access memory (RAM) and a cache, wherein said cache enables
10 faster access to data to a processing unit, said determining a
11 minimum duration further comprises determining an additional time
12 required by said pipelined screening if a data structure for a
13 desired tile size does not fit in said cache, wherein said data
14 structure is used in said pipelined screening.

1 39. (New) The method of claim 32, wherein:
2 said determining a minimum duration of time consumed by
3 either said back-end screening or said pipelined screening
4 calculates CLK as follows:

5
$$CLK = T_d - T_p - T_c$$

6 where T_d is the additional time required for back-end
7 screening given by:

8
$$T_d = (\text{Pagesize} \times \text{DPSI}) \times 2 / (\text{Transfer-rate})$$

9 where: Pagesize is the area of the page; DPSI is the dots per
10 square inch; and Transfer-rate is a memory data transfer rate;
11 where T_p is the difference in screening performance between
12 pipeline screening and back-end screening given by:

13
$$T_p = (\sum A_i \times DPSI \times CLK_p) - (Pagesize \times DPSI \times CLK_b)$$

14 where: A_i is the bounding box area of i^{th} display list element i
15 in square inches; CLK_p is the average number clock cycles
16 required to process each pixel in pipeline screening; and CLK_b is
17 the average number clock cycles required to process each pixel in
18 back-end screening;

19 where T_c is the difference in cache misses between pipeline
20 screening back-end screening given by:

21
$$T_c = (\sum (I_n \times (C_{pi} - C_{bi}))) \times CLK_{cache}$$

22 where: I_n is the total number of element of type i in the display
23 list; C_{pi} is the number of cache misses in one rendering for an
24 element of type i in pipeline screening; C_{bi} is the number of
25 cache misses in one rendering for element type i in back-end
26 screening; and CLK_{cache} is the number of clock cycles required to
27 serve one cache miss.

1 40. (New) The method of claim 32, wherein:
2 said determining a minimum duration of time consumed by
3 either said back-end screening or said pipelined screening
4 employing a predetermined screen tile height in screening
5 calculates CLK as follows:

6
$$CLK = T_d - T_p - T_c - T_t$$

7 where T_d is the additional time required for back-end
8 screening given by:

9 $T_d = (\text{Pagesize} \times \text{DPSI}) \times 2 / (\text{Transfer-rate})$

10 where: Pagesize is the area of the page; DPSI is the dots per
11 square inch; and Transfer-rate is a memory data transfer rate;
12 where T_p is the difference in screening performance between
13 pipeline screening and back-end screening given by:

14 $T_p = (\sum A_i \times \text{DPSI} \times \text{CLK}_p) - (\text{Pagesize} \times \text{DPSI} \times \text{CLK}_b)$

15 where: A_i is the bounding box area of i^{th} display list element i
16 in square inches; CLK_p is the average number clock cycles
17 required to process each pixel in pipeline screening; and CLK_b is
18 the average number clock cycles required to process each pixel in
19 back-end screening;

20 where T_c is the difference in cache misses between pipeline
21 screening back-end screening given by:

22 $T_c = (\sum (I_n \times (C_{pi} - C_{bi}))) \times \text{CLK}_{\text{cache}}$

23 where: I_n is the total number of element of type i in the display
24 list; C_{pi} is the number of cache misses in one rendering for an
25 element of type i in pipeline screening; C_{bi} is the number of
26 cache misses in one rendering for element type i in back-end
27 screening; and $\text{CLK}_{\text{cache}}$ is the number of clock cycles required to
28 serve one cache miss; and

29 where: T_t is the number of excess clock cycles between
30 pipelined screening and back-end screening due to a screening

31 table not being able to fit in a cache when the object height is
32 less than the predetermined screen tile height given by:

33
$$T_t = (\sum a_i \times DPSI) \times CLK_{tp}$$

34 where: a_i is bounding box area of display list element i ; and
35 CLK_{tp} is the number of clock cycles to process a cache miss.

1 41. (New). The method of claim 32, wherein:
2 said determining a minimum duration of time consumed by
3 either said back-end screening or said pipelined screening
4 employing a predetermined screen tile height in screening
5 calculates CLK as follows:

6
$$CLK = T_d - T_p - T_c - T_t$$

7 where T_d is the additional time required for back-end
8 screening given by:

9
$$T_d = (Pagesize \times DPSI) \times 2 / (\text{Transfer-rate})$$

10 where: Pagesize is the area of the page; DPSI is the dots per
11 square inch; and Transfer-rate is a memory data transfer rate;
12 where T_p is the difference in screening performance between
13 pipeline screening and back-end screening given by:

14
$$T_p = (\sum A_i \times DPSI \times CLK_p) - (Pagesize \times DPSI \times CLK_b)$$

15 where: A_i is the bounding box area of i^{th} display list element i
16 in square inches; CLK_p is the average number clock cycles
17 required to process each pixel in pipeline screening; and CLK_b is

18 the average number clock cycles required to process each pixel in
19 back-end screening;

20 where T_c is the difference in cache misses between pipeline
21 screening back-end screening given by:

22
$$T_c = (\sum (I_n \times (C_{pi} - C_{bi}))) \times CLK_{cache}$$

23 where: I_n is the total number of element of type i in the display
24 list; C_{pi} is the number of cache misses in one rendering for an
25 element of type i in pipeline screening; C_{bi} is the number of
26 cache misses in one rendering for element type i in back-end
27 screening; and CLK_{cache} is the number of clock cycles required to
28 serve one cache miss; and

29 where: T_t is the number of excess clock cycles between
30 pipelined screening and back-end screening due to a screening
31 table not being able to fit in a cache when the object height is
32 greater than the predetermined screen tile height given by:

33
$$T_t = (\sum h_i \times DPSI \times T_w) \times CLK_{tp}$$

34 where: h_i is the height of display list element i ; T_w is the width
35 of the screen; and CLK_{tp} is the number of clock cycles to process
36 a cache miss.

1 42. (New) A system for generating an image using raster
2 image processing, said image being generated based on a
3 specification specifying said image, said specification
4 containing data representing a plurality of objects in a page,
5 said system comprising:

6 means for implementing a plurality of approaches, with each
7 approach being designed to generate said image;

8 means for receiving said specification;
9 means for examining said specification to determine a number
10 of resources required to generate said image of a subset of a
11 page including plural objects in each of said plurality of
12 approaches;
13 means for selecting one of said plurality of approaches
14 which requires an optimal number of resources;
15 means for generating said image of said page from said
16 specification using said selected one of said plurality of
17 approaches.

1 43. (New) The method of claim 42, wherein:
2 said subset of a page including plural objects consists of a
3 band of a predetermined number of adjacent horizontal lines.

1 44. (New) The method of claim 42, wherein:
2 said subset of a page including plural objects consists of a
3 subband of a rectangle of a predetermined number of adjacent
4 pixels in a predetermined number of adjacent horizontal lines.

1 45. (New) The system of claim 42, further comprising:
2 a random access memory (RAM);
3 a cache, wherein said cache enables faster access to data to
4 a processing unit;
5 wherein said plurality of approaches includes rendering and
6 screening via back-end screening and rendering and screening via
7 pipelined screening;
8 wherein said means for examining comprises means for
9 determining a minimum duration of time consumed by either said
10 back-end screening or said pipelined screening; and

11 wherein said means for determining a minimum duration
12 further comprises means for determining an additional time
13 required by said back-end screening approach due to storing
14 rendered data in said RAM.

1 46. (New) The method of claim 42, wherein:
2 said means for determining a minimum duration further
3 comprises means for determining an additional time required by
4 said pipelined screening due to the overlap of objects contained
5 in said specification for said image.

1 47. (New) The method of claim 42, further comprising:
2 a random access memory (RAM);
3 a cache, wherein said cache enables faster access to data to
4 a processing unit than said random access memory; and
5 wherein said means for determining a minimum duration
6 further comprises means for determining an additional time
7 required by said pipelined screening when said processing unit
8 accesses a code in cache enabling implementation of said
9 pipelined screening, and an instruction cache miss results in
10 accessing said code in said cache.

1 48. (New) The method of claim 42, further comprising:
2 a random access memory (RAM);
3 a cache, wherein said cache enables faster access to data to
4 a processing unit than said random access memory (RAM); and
5 wherein said means for determining a minimum duration
6 further comprises means for determining an additional time
7 required by said pipelined screening if a data structure for a
8 desired tile size does not fit in said cache, wherein said data
9 structure is used in said pipelined screening.

1 49. (New) The method of claim 42, wherein:
2 said determining a minimum duration of time consumed by
3 either said back-end screening or said pipelined screening
4 calculates CLK as follows:

5 $CLK = T_d - T_p - T_c$

6 where T_d is the additional time required for back-end
7 screening given by:

8 $T_d = (\text{Pagesize} \times \text{DPSI}) \times 2 / (\text{Transfer-rate})$

9 where: Pagesize is the area of the page; DPSI is the dots per
10 square inch; and Transfer-rate is a memory data transfer rate;

11 where T_p is the difference in screening performance between
12 pipeline screening and back-end screening given by:

13 $T_p = (\sum A_i \times \text{DPSI} \times CLK_p) - (\text{Pagesize} \times \text{DPSI} \times CLK_b)$

14 where: A_i is the bounding box area of i^{th} display list element i
15 in square inches; CLK_p is the average number clock cycles
16 required to process each pixel in pipeline screening; and CLK_b is
17 the average number clock cycles required to process each pixel in
18 back-end screening;

19 where T_c is the difference in cache misses between pipeline
20 screening back-end screening given by:

21 $T_c = (\sum (I_n \times (C_{pi} - C_{bi}))) \times CLK_{\text{cache}}$

22 where: I_n is the total number of element of type i in the display
23 C_{pi} is the number of cache misses in one rendering for an
24 element of type i in pipeline screening; C_{bi} is the number of
25 cache misses in one rendering for element type i in back-end
26 screening; and CLK_{cache} is the number of clock cycles required to
27 serve one cache miss.

1 50. (New) The method of claim 42, wherein:
2 said determining a minimum duration of time consumed by
3 either said back-end screening or said pipelined screening
4 employing a predetermined screen tile height in screening
5 calculates CLK as follows:

6 $CLK = T_d - T_p - T_c - T_t$

7 where T_d is the additional time required for back-end
8 screening given by:

9 $T_d = (\text{Pagesize} \times \text{DPSI}) \times 2 / (\text{Transfer-rate})$

10 where: Pagesize is the area of the page; DPSI is the dots per
11 square inch; and Transfer-rate is a memory data transfer rate;
12 where T_p is the difference in screening performance between
13 pipeline screening and back-end screening given by:

14 $T_p = (\sum A_i \times \text{DPSI} \times \text{CLK}_p) - (\text{Pagesize} \times \text{DPSI} \times \text{CLK}_b)$

15 where: A_i is the bounding box area of i^{th} display list element i
16 in square inches; CLK_p is the average number clock cycles
17 required to process each pixel in pipeline screening; and CLK_b is

18 the average number clock cycles required to process each pixel in
19 back-end screening;

20 where T_c is the difference in cache misses between pipeline
21 screening back-end screening given by:

22
$$T_c = (\sum (I_n \times (C_{pi} - C_{bi}))) \times CLK_{cache}$$

23 where: I_n is the total number of element of type i in the display
24 list; C_{pi} is the number of cache misses in one rendering for an
25 element of type i in pipeline screening; C_{bi} is the number of
26 cache misses in one rendering for element type i in back-end
27 screening; and CLK_{cache} is the number of clock cycles required to
28 serve one cache miss; and

29 where: T_t is the number of excess clock cycles between
30 pipelined screening and back-end screening due to a screening
31 table not being able to fit in a cache when the object height is
32 less than the predetermined screen tile height given by:

33
$$T_t = (\sum a_i \times DPSI) \times CLK_{tp}$$

34 where: a_i is bounding box area of display list element i ; and
35 CLK_{tp} is the number of clock cycles to process a cache miss.

1 51. (New) The method of claim 42, wherein:

2 said determining a minimum duration of time consumed by
3 either said back-end screening or said pipelined screening
4 employing a predetermined screen tile height in screening
5 calculates CLK as follows:

6
$$CLK = T_d - T_p - T_c - T_t$$

7 where T_d is the additional time required for back-end
8 screening given by:

9 $T_d = (\text{Pagesize} \times \text{DPSI}) \times 2 / (\text{Transfer-rate})$

10 where: Pagesize is the area of the page; DPSI is the dots per
11 square inch; and Transfer-rate is a memory data transfer rate;

12 where T_p is the difference in screening performance between
13 pipeline screening and back-end screening given by:

14 $T_p = (\sum A_i \times \text{DPSI} \times \text{CLK}_p) - (\text{Pagesize} \times \text{DPSI} \times \text{CLK}_b)$

15 where: A_i is the bounding box area of i^{th} display list element i
16 in square inches; CLK_p is the average number clock cycles
17 required to process each pixel in pipeline screening; and CLK_b is
18 the average number clock cycles required to process each pixel in
19 back-end screening;

20 where T_c is the difference in cache misses between pipeline
21 screening back-end screening given by:

22 $T_c = (\sum (I_n \times (C_{pi} - C_{bi}))) \times \text{CLK}_{\text{cache}}$

23 where: I_n is the total number of element of type i in the display
24 list; C_{pi} is the number of cache misses in one rendering for an
25 element of type i in pipeline screening; C_{bi} is the number of
26 cache misses in one rendering for element type i in back-end
27 screening; and $\text{CLK}_{\text{cache}}$ is the number of clock cycles required to
28 serve one cache miss; and

29 where: T_t is the number of excess clock cycles between
30 pipelined screening and back-end screening due to a screening

31 table not being able to fit in a cache when the object height is
32 greater than the predetermined screen tile height given by:

33
$$T_t = (\sum h_i \times DPSI \times T_w) \times CLK_{tp}$$

34 where: h_i is the height of display list element i ; T_w is the width
35 of the screen; and CLK_{tp} is the number of clock cycles to process
36 a cache miss.